REMARKS

In response to the Office Action mailed on June 8th, 2007, Applicant wishes to enter the following remarks for the Examiner's consideration. Claims 6, 7 and 10-15 are pending in the application.

Rejection of claims under 35 USC §103

Claims 6, 10, 11 and 12 have been rejected under 35 USC §103(a) as being unpatentable over Tanaka (Patent No. US 5,893,143) in view of Limberis et al. (Patent No. US 5,852,729). Applicant respectfully traverses this rejection of the claims.

The Examiner acknowledges that the Tanaka reference fails to teach, disclose or suggest the recitation of the claims, and relies upon the teachings of Limberis to overcome this defect.

While Applicant agrees that the Tanaka reference fails to teach the use of an identifier to indicate that an ordered field contains a NOP in every control word of sequence, Applicant must take exception with the characterization by the Examiner that the Limberis teaches, discloses or suggests this element of the claim. Combination of the Limberis reference with the Tanaka reference does not cure this defect and thus the combination fails to yield the recitations of the claims. Applicant therefore respectfully submits that this grounds of rejection is improper and should be withdrawn.

Claim 6 is a method for a processor to process a sequence of a plurality of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for a corresponding element of the processor. Limberis does not disclose a processor for processing control words comprising a plurality of ordered fields, so there is no motivation to combine Limberis with Tanaka in the first place.

The first element of claim 6 calls for fetching an identifier having one bit for each element of the processor, wherein a bit of the identifier is set if a corresponding ordered field contains a NOP instruction in every control word of the sequence of control words. This is not disclosed by Limberis. The NOP flags of Limberis do not correspond to elements of the processor or the corresponding ordered fields of a multi-instruction field. Limberis uses NOP

flag to replace a program of instructions in a microcode store. The NOP flag of Limberis relates to the program instruction which is to be replaced and is asserted if the program is to be replaced. The NOP flag of Limberis has only a single bit and it is unrelated to the particular instruction of the control word. In contrast the identifier of claim 6 has one bit for each element of the processor. For example, column 9, lines 20-23, states that when the NOP flag is not asserted the instruction is executed normally, but when it is asserted the instructions are overwritten. Thus, even if the instruction is not a NOP, it is overwritten. Limberis, column 9, lines 23-26, say that this prevents the instructions from changing register values. In claim 6, the identifiers only identify ordered fields containing NOPs – these instructions do not change register values.

Claim 6 also calls for disabling an element of the processor, to reduce power consumption by the processor, if a corresponding bit of the identifier is set. This is not taught by Limberis. Limberis teaches replacing one program with another program. The processor is not disabled and the power consumption is not reduced.

In summary, the NOP flag of Limberis is not equivalent to the identifier of claim 6 since:

(1) The NOP flag has only one bit (or one bit for each instruction of a sequence), whereas the identifier of claim 6 has one bit for each processor element of the processor and indicates that an ordered field contains a NOP in every control word of a sequence.

(2) The NOP flag identifies a program instruction to be overwritten and is independent of the contents of the instruction, whereas the identifier of claim 6 identifies a processing element to be disabled and is dependent upon the location of NOPs in the complete sequence of multi-instruction words.

(3) Limberis uses one NOP flag for each instruction word of a sequence, whereas claim 6 has a single identifier for the complete sequence (the number of bits in the identifier is not dependent on the number of control words in the sequence).

Similarly, the examiner has agreed that the mask of Tanaka does not indicate that an ordered field contains a NOP in every control word of sequence. Therefore, Applicant respectfully submits that the Tanaka and Limberis references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the use of an identifier having one bit for each processor element of the processor and indicates that an ordered field contains a NOP in every control word of a sequence. Both Limberis and Tanaka have one identifier for each control word of a sequence, whereas claim 6 has a single identifier for the whole sequence.

Claim 7 depends from claim 6, discussed above, and also calls for disabling a memory bank of the plurality of memory banks while the sequence of control words is processed, to reduce power consumption by the processor further, if a corresponding bit of the identifier is set. This element of the claim is not taught by Limberis.

Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claims 6 and 7 be mailed at the Examiner's earliest convenience.

Claim 10 calls for a mask latch for storing a compression mask having one bit for each element of the processor, wherein a bit of the compression mask is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of control words. As discussed above with reference to claim 6, such a compression mask is not taught, disclosed or otherwise suggest by Limberis, Tanaka or any combination thereof. In particular, both Limberis and Tanaka have one identifier for each control word of a sequence, whereas claim 6 has a single identifier for the whole sequence.

Claims 11 and 12 depend from claim 10. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. Applicant thus respectfully requests that this basis of rejection of the claims be withdrawn and that a Notice of Allowance for claim 10, 11 and 12 be mailed at the Examiner's earliest convenience.

Claim 13 has been rejected under 35 USC §103(a) as being unpatentable over Tanaka (US 5,893,143) in view of Limberis et al. (Patent No. US 5,852,729) and further in view of Pechanek et al. (US 6,173,389). Applicant respectfully traverses this rejection of the claims.

The Examiner acknowledges that no combination of the Tanaka and Limberis reference teach, disclose or suggest the recitation of claim 13, and relies upon the teachings of Pechanek to overcome this defect.

Claim 13 depends from claim 12 discussed above. Applicant submits, in light of the foregoing discussion of claim 10, that even if one were to combine the Tanaka and Limbers references with the Pechanek reference, the result would not be the claimed invention of claim 13. Claim 10, from which claim 13 depends, calls for a mask latch for storing a compression mask having one bit for each element of the processor, wherein a bit of the compression mask is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of control words. As discussed above with reference to claim 6, such a compression mask is not taught, disclosed or otherwise suggested by Limberis, Tanaka or any combination thereof. In particular, both Limberis and Tanaka have one identifier for each control word of a sequence, whereas claim 6 has a single identifier for the whole sequence. This defect is not cured by the Pechanek reference, which does not disclose a compression mask.

Further, neither Tanaka nor Limberis teach a system in which datapath elements are disabled for execution of a complete sequence of control words (as recited by claim 12 from which claim 13 depends). This defect is not cured by the Pechanek reference.

In light of the foregoing remarks, Applicant respectfully submits that the Tanaka, Limberis and Pachanek references, whether considered alone or in combination fail to teach, disclose, suggest or otherwise render obvious the recitations of claim 13. Applicant thus respectfully requests that this basis of rejection of the claim be withdrawn and that a Notice of Allowance for claim 13 be mailed at the Examiner's earliest convenience.

Claims 7 and 14 has been rejected under 35 USC §103(a) as being unpatentable over Tanaka (Patent No. US 5,893,143) in view of Limberis (Patent No. US 5,852,729) in view of Shebanow (Patent No. US 5,367,494). Applicant respectfully traverses this rejection of the claims.

Claim 7 has been discussed above in relation to the Tanaka and Limberis patents. Claim 7, which depends from claim 6, introduces the further element of disabling a memory bank associated with a datapath element for every control word in the sequence if a corresponding bit of a single identifier is set. In Tanaka, a mask bit corresponds to a particular instruction. Even if one were to use Tanaka's mask to disable a datapath element, it would only be disabled for one instruction, not for the whole sequence. For example, if the first instruction of sequence had a NOP is the second field, a corresponding datapath element could be disabled for one instruction, but it could not be disabled for the whole sequence, because the identifier does not indicate whether subsequent instruction will have NOPs in the second field.

This defect is not cured by the Limberis reference, since the NOP flag gives no indication as to whether subsequent instructions of a sequence should be executed or overwritten. Neither is this defect cured by the Shebanow reference.

Similarly, in **claim 14**, datapath elements and memory banks are disabled before the sequence of control word is processed. In Tanaka, each control word and its associated mask is processed separately. Thus, in Tanaka, the configuration is altered as the sequence of control word is processed, not before. This is also true of the Limberis reference, where the NOP flag gives no indication of whether future instructions are to be executed or overwritten. Thus, neither approach would allow datapath elements to be disabled in advance.

This defect is not cured by the Shebanow reference.

Claim 15 depends from claim 14. Although additional arguments could be made for the patentability of claim 15, such arguments are believed unnecessary in view of the above discussion. Further, It is noted for the

record that the combination of the Tanaka, Limberis et al, Shebanow et al., and Pechanek et al. references fail to yield the claimed invention of claim 14, from which claim 15 depends, as discussed above.

In light of the foregoing amendments and explanations, applicant submits that all rejections of claims 6, 7 and 10-15 have been overcome. Allowance of claims 6, 7 and 10-15 is therefore respectfully requested at the Examiner's earliest convenience. Although additional arguments could be made for the patentability of each of the claims, such arguments are believed unnecessary in view of the above discussion. The undersigned wishes to make it clear that not making such arguments at this time should not be construed as a concession or admission to any statement in the Office Action.

Please contact the undersigned if you have any questions regarding this application.

Respectfully submitted,

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